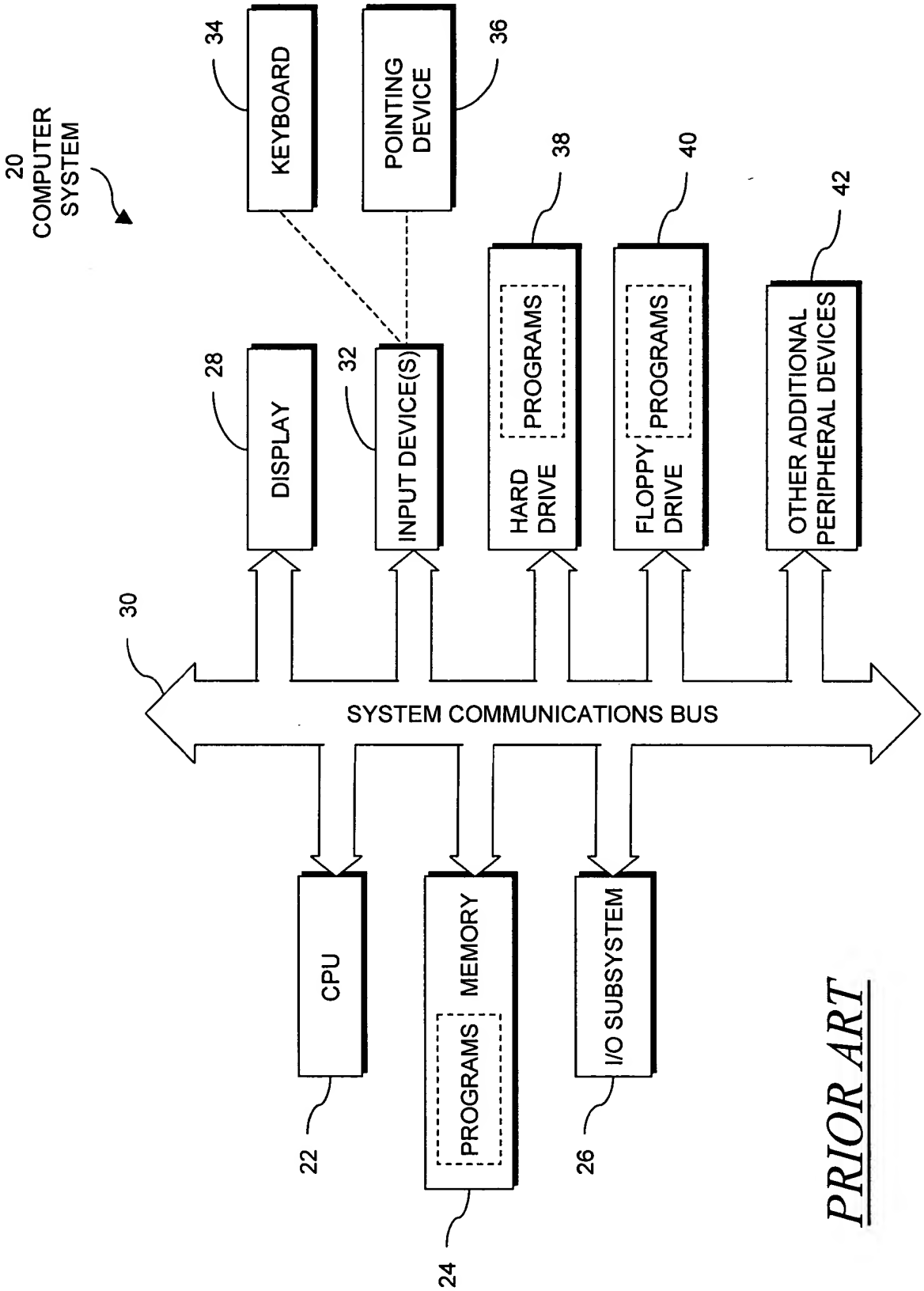

FIG. 1

PRIOR ART

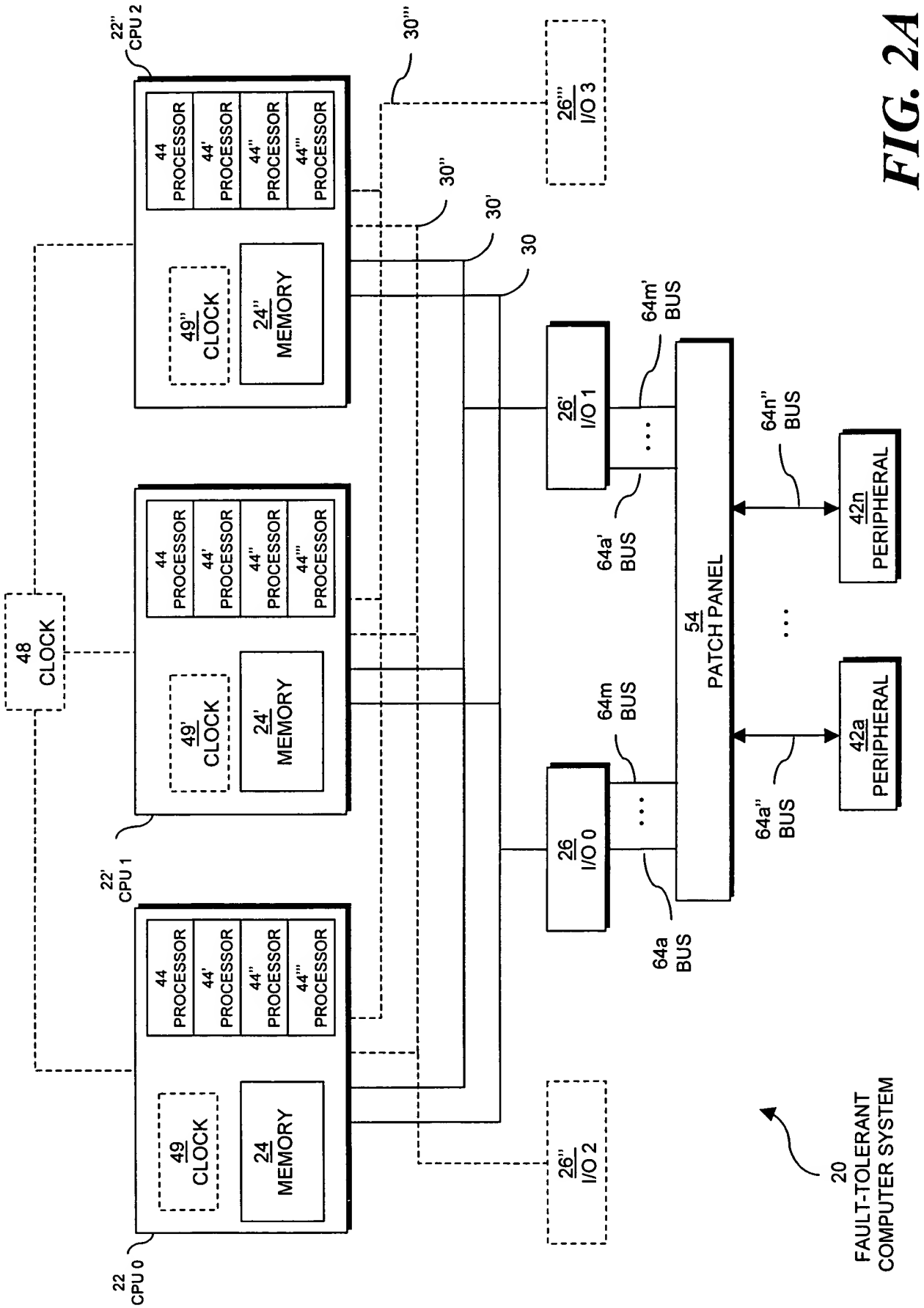
22" CPU 2
44 PROCESSOR
44' PROCESSOR
44" PROCESSOR
44"' PROCESSOR
49" CLOCK
24" MEMORY
30"'
26"' I/O 3
30"
30'
30
64m' BUS
26' I/O 1
64a' BUS
64n" BUS
42n PERIPHERAL
48 CLOCK
49' CLOCK
24' MEMORY
22' CPU 1
64m BUS
54 PATCH PANEL
26 I/O 0
64a BUS
64a" BUS
42a PERIPHERAL
49 CLOCK
24 MEMORY
26" I/O 2
22 CPU 0
20 FAULT-TOLERANT COMPUTER SYSTEM

FIG. 2A

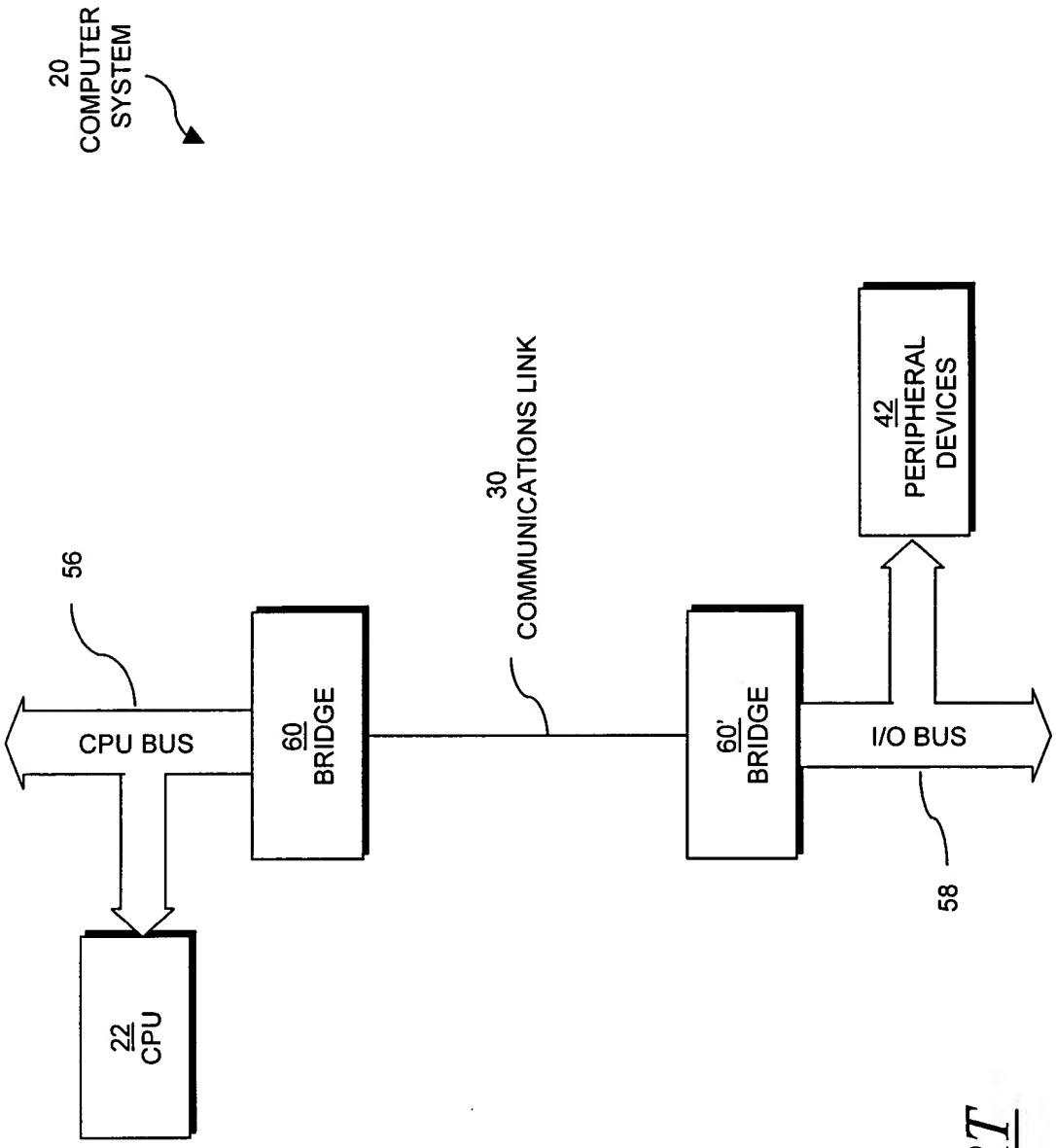

FIG. 2B

PRIOR ART

10020-20020

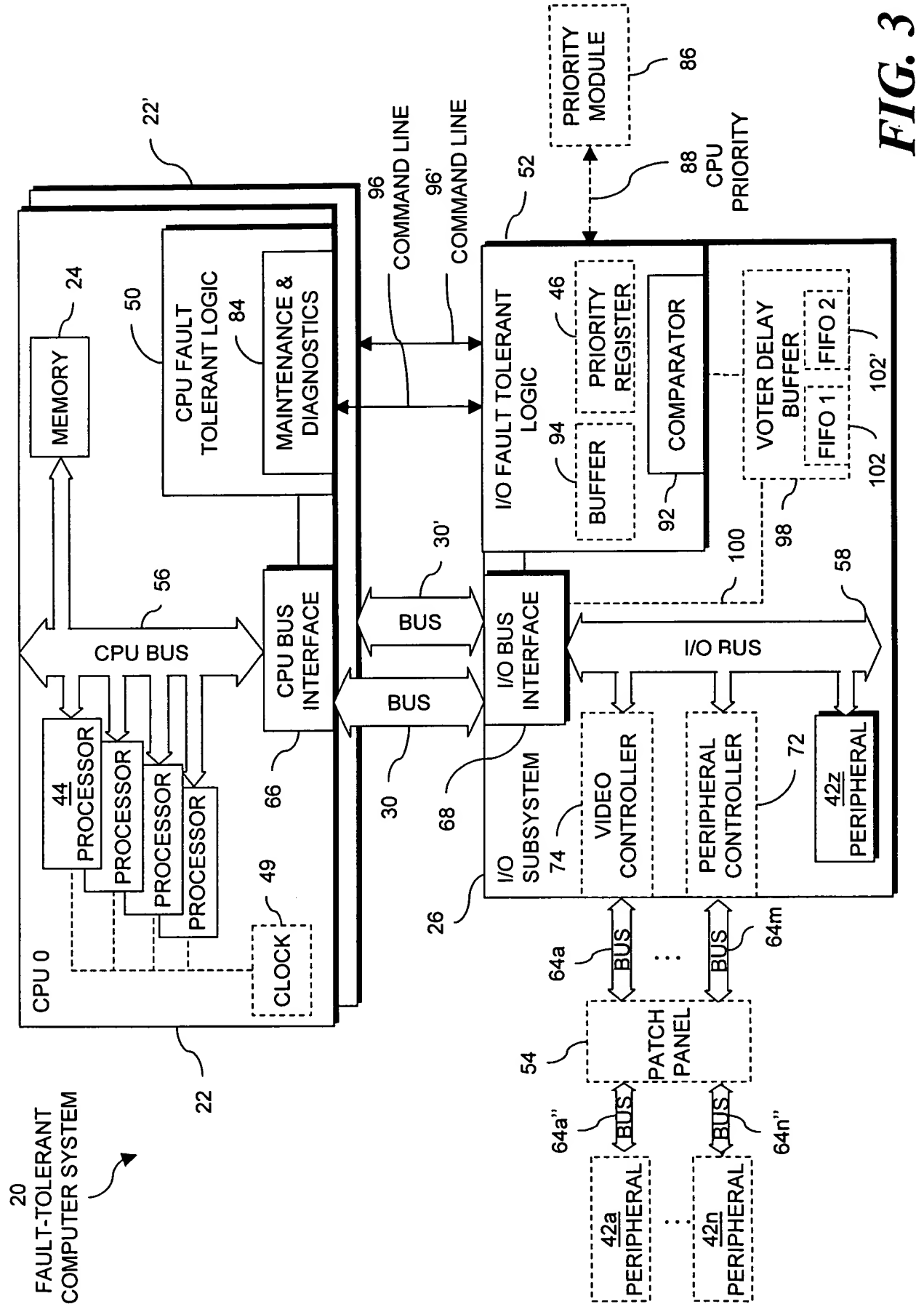

FIG. 3

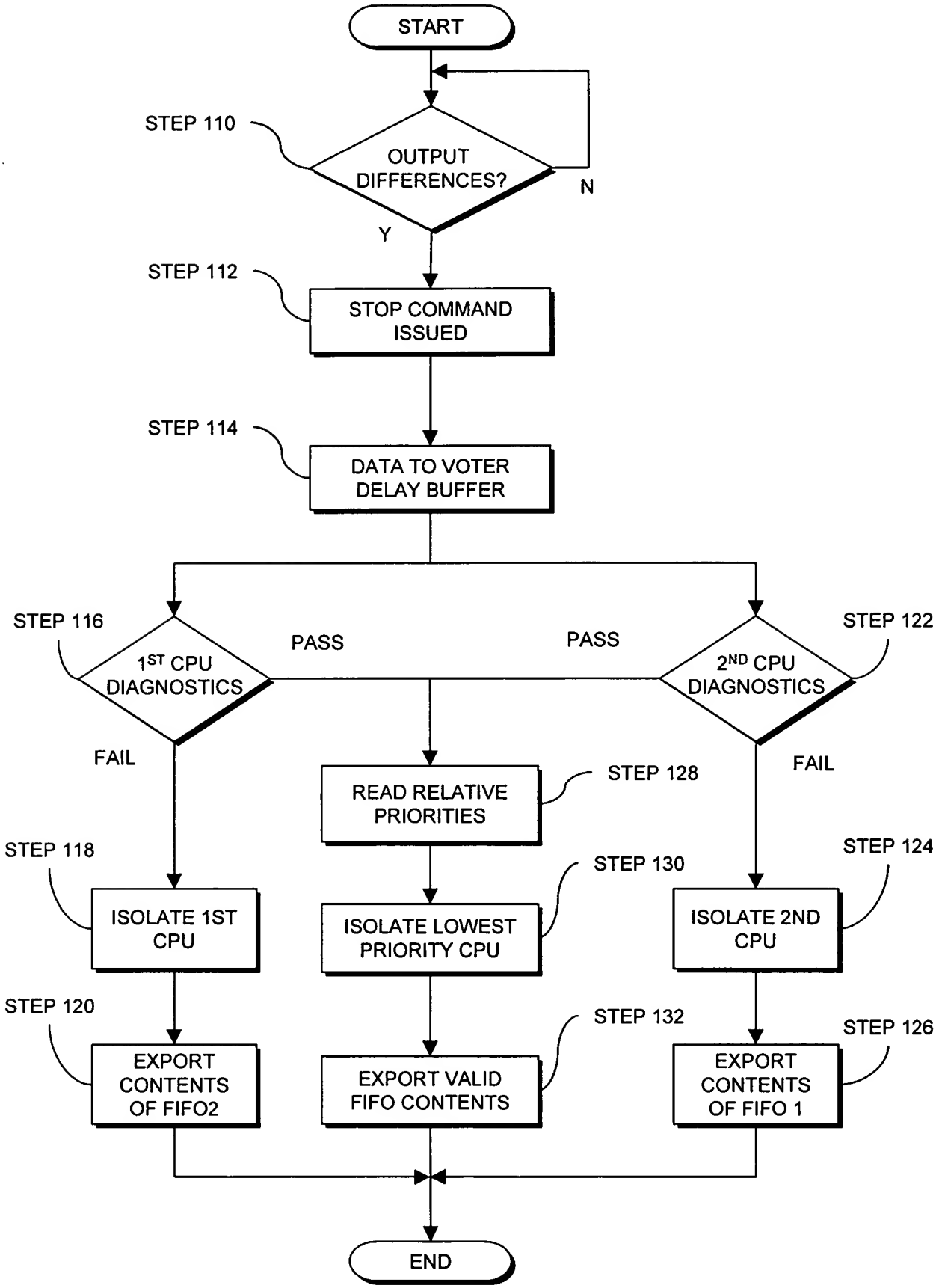
START
STEP 110
OUTPUT DIFFERENCES?
N
Y
STEP 112
STOP COMMAND ISSUED
STEP 114
DATA TO VOTER DELAY BUFFER
STEP 116
1ST CPU DIAGNOSTICS
PASS
PASS
STEP 122
2ND CPU DIAGNOSTICS
FAIL
FAIL
READ RELATIVE PRIORITIES
STEP 128
STEP 118
ISOLATE 1ST CPU
STEP 130
ISOLATE LOWEST PRIORITY CPU
STEP 124
ISOLATE 2ND CPU
STEP 120
EXPORT CONTENTS OF FIFO2
STEP 132
EXPORT VALID FIFO CONTENTS
STEP 126
EXPORT CONTENTS OF FIFO 1
END

FIG. 4

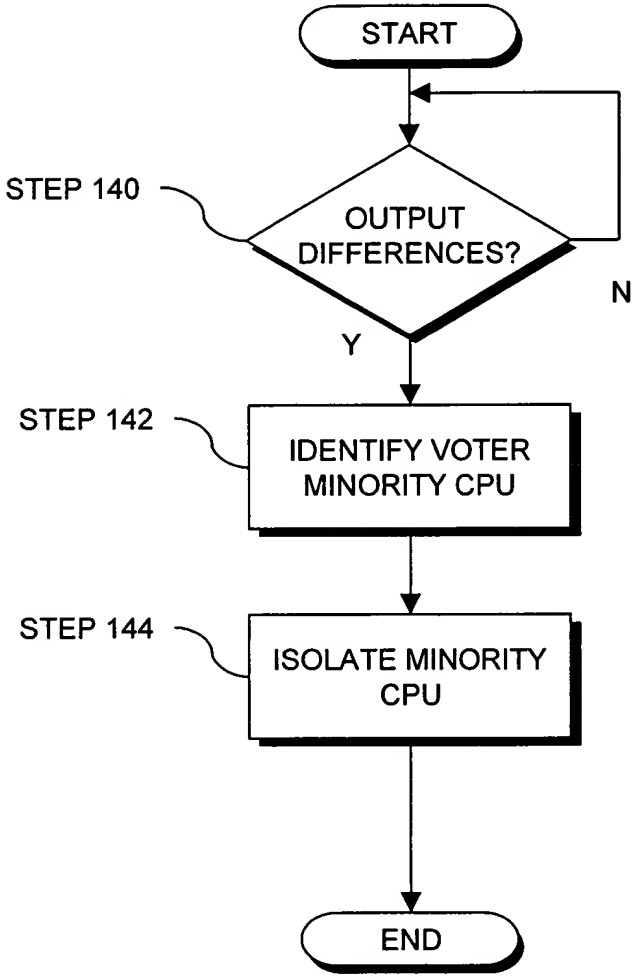
START
STEP 140
OUTPUT DIFFERENCES?
N
Y
STEP 142
IDENTIFY VOTER MINORITY CPU
STEP 144
ISOLATE MINORITY CPU
END

FIG. 5

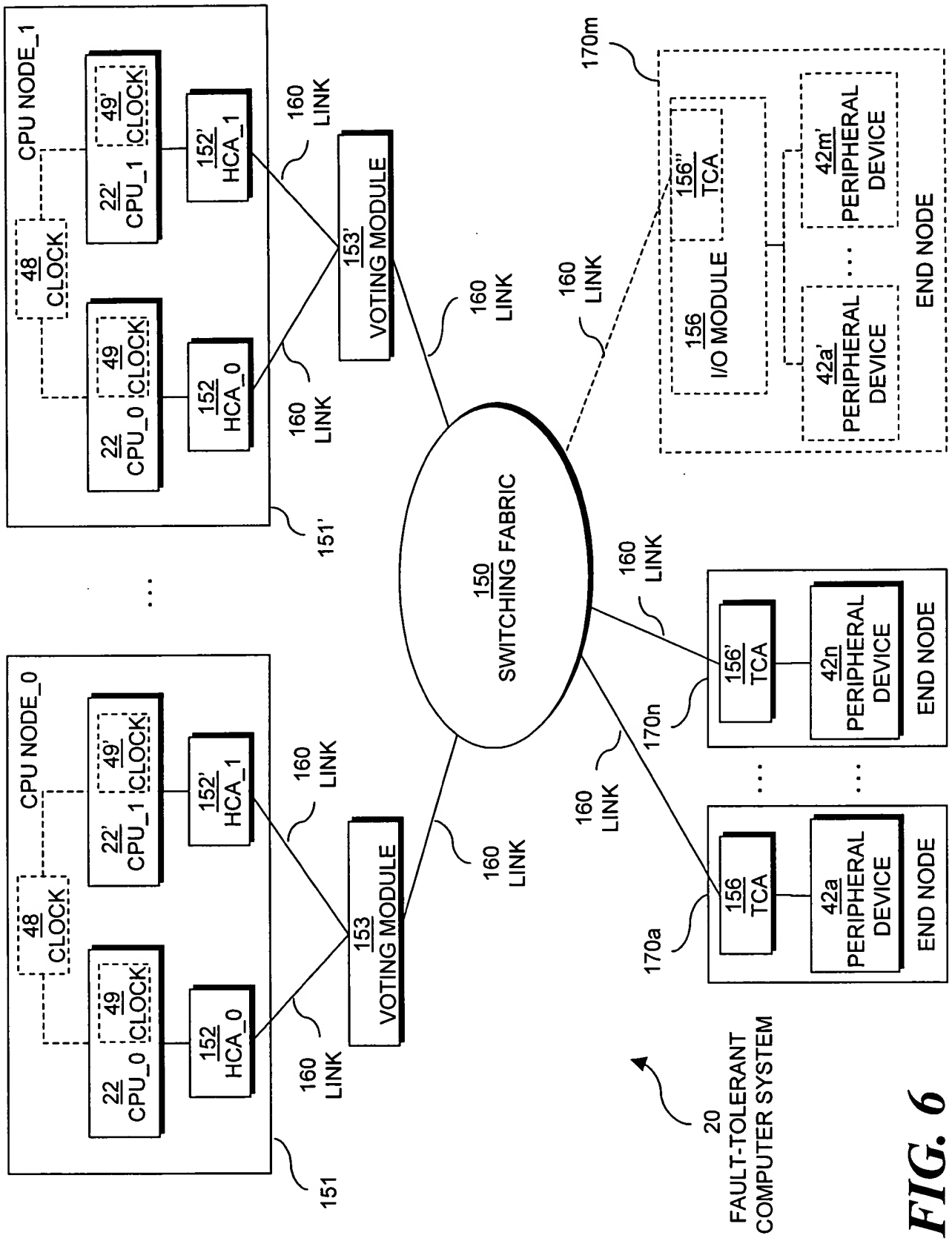
CPU NODE_1
48 CLOCK
22 CPU_0
49 CLOCK
152 HCA_0
22' CPU_1
49' CLOCK
152' HCA_1
151'
160 LINK
153' VOTING MODULE
CPU NODE_0
48 CLOCK
22 CPU_0
49 CLOCK
152 HCA_0
22' CPU_1
49' CLOCK
152' HCA_1
151
153 VOTING MODULE
150 SWITCHING FABRIC
170m
156'' TCA
156 I/O MODULE
42a' PERIPHERAL DEVICE
42m' PERIPHERAL DEVICE
END NODE
170n
156' TCA
42n PERIPHERAL DEVICE
END NODE
170a
156 TCA
42a PERIPHERAL DEVICE
END NODE
20 FAULT-TOLERANT COMPUTER SYSTEM

FIG. 6

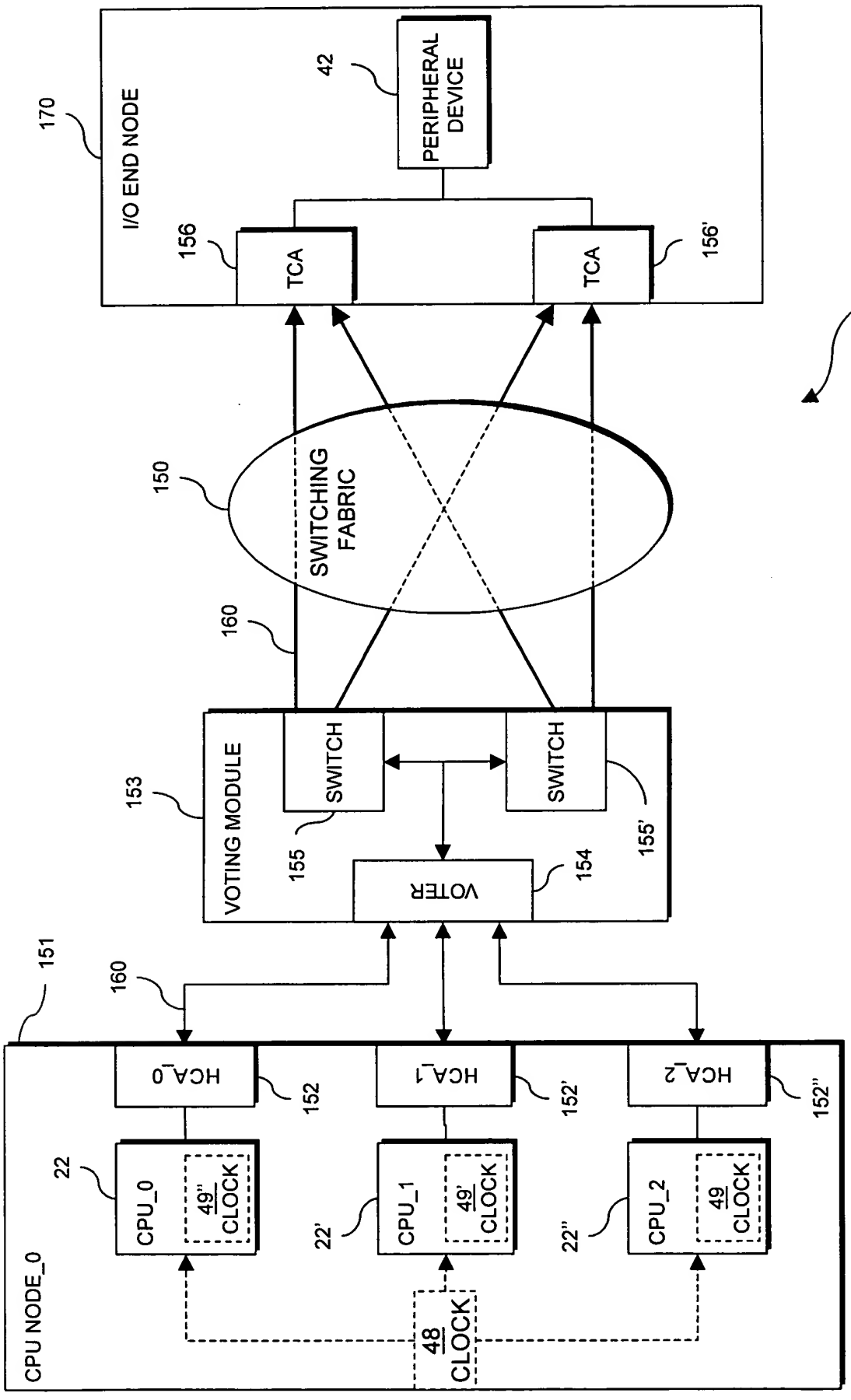
20
FAULT-TOLERANT COMPUTER SYSTEM
170
I/O END NODE
42
PERIPHERAL DEVICE
156
TCA
156'
TCA
150
SWITCHING FABRIC
160
153
VOTING MODULE
SWITCH
155
SWITCH
155'
VOTER
154
151
160
CPU NODE_0
HCA_0
152
HCA_1
152'
HCA_2
152''
22
CPU_0
49'' CLOCK
22'
CPU_1
49' CLOCK
22''
CPU_2
49 CLOCK
48 CLOCK

FIG. 7